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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/750,093	12/31/2003	Jung-Bae Lee	9898-324	1914

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EXAMINER
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TRAN, ANDREW Q

ART UNIT	PAPER NUMBER
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2824

DATE MAILED: 05/15/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

## Office Action Summary

**Application No.**

10/750,093

**Applicant(s)**

LEE ET AL.

**Examiner**

Andrew Q. Tran

**Art Unit**

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 07 February 2006.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-42 is/are pending in the application.
- 4a) Of the above claim(s) 7-14, 21-38 and 40-42 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-6, 15-20 and 39 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 31 December 2003 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
- 1) ☒ Certified copies of the priority documents have been received.
  - 2) ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - 3) ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date 12/31/03 & 8/23/05
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_

## DETAILED ACTION

### *Election/Restrictions*

Applicant's election without traverse of Group I invention and Species A of Figs. 5-6 (claims 1-6, 15-20 and 39) in the reply filed on February 07, 2006 is acknowledged.

Claims 1, 15 and 39 are generic to all disclosed embodiments.

Claims 7-14, 21-38 and 40-42 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention/species, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on February 07, 2006.

### *Drawings*

The drawings are objected to because :

Figs. 1, 3 and 4 should be labeled as --PRIOR ART--, as disclosed in the instant specification. In Fig. 1, circuit block 104 should be relabeled as --Memory Controller--. In Fig. 2, reference numeral "114" on the left side of Memory Module MD1 should be deleted. Further, in Fig. 2, circuit block 104 should be relabeled as --Memory Controller--. In Fig. 6, circuit block 504 should be relabeled as --Memory Controller--. In Fig. 7, circuit block 504 should be relabeled as --Memory Controller--. In Fig. 8, circuit block 504 should be relabeled as --Memory Controller--.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing

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should not be labeled as “amended.” If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either “Replacement Sheet” or “New Sheet” pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

### ***Specification***

The disclosure is objected to because of the following informalities:

The instant specification contains numerous typographical errors, especially in the reference numerals. Examples of such errors are : at page 5, line 3-4, “controller 704” should have been --controller 504--; or at page 6, line 3, “memory module 706” should have been --memory module 716--.

Appropriate correction is required.

### ***Claim Objections***

Claims 1, 4, 17-18 and 39 are objected to because of the following informalities:

In claim 1, line 3, “to” (second occurrence) should be changed to --on--. In claim 4, line 6, “perpendicularly with” should be changed to --perpendicular to--. In claim 17, line 1, “at least one” should be deleted. In claim 18, line 3, “at least one” should be deleted; at line 6, “perpendicularly with” should be changed to --perpendicular to--; and --. (the period) should be

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added to the end of the line. In claim 39, line 6, "to" (second occurrence) should be changed to --on--.

Appropriate correction is required.

### ***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-4, 15-18 and 39 are rejected under 35 U.S.C. 102(b) as being anticipated by Akimoto (US Pat 5,321,664 hereafter "Akimoto"). See for example, Figs. 1, 3 and 9.

As to claim 1, Akimoto discloses in Fig. 1, a memory system comprising a first buffer (input buffer 1B) mounted on a motherboard (substrate SUB); at least one first memory device (RAM1) coupled to the first buffer and mounted on the motherboard; and a plurality of signal traces (read select signals RS, write select signals WS, internal write select signals ws) routed on the motherboard to the first buffer and the at least one first memory device. As to claim 2, the first buffer (input buffer 1B) drives the at least one first memory device with address signals (address signal a0-ai) and command signals (read select signals RS, write select signals WS). As to claim 4, note the first signal traces RS and WS are perpendicular to second signal traces ws.

Claims 15-18 and 39 are similarly rejected on same grounds. As to claim 39, note in particular that "a memory controller" is inherent in Akimoto's memory system for controlling the memory system.

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***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 5-6 and 19-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Akimoto.

Akimoto discloses a memory system as shown in Fig. 1 above, comprising all claimed features.

Akimoto fails to disclose a memory system where the at least one first memory device is a SDRAM.

However synchronous dynamic random access memory (SDRAM) working in conjunction with a system clock signal is well known in the art.

Therefore it would have been obvious to a person having ordinary skill in the art at the time the invention was made to incorporate the DRAM into Akimoto's memory system because such incorporation would enhance the operation speed of the memory system thanks to the system clock signal.

***Conclusion***

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Matsui (US Pat 6,917,546) describes a memory device and a memory system.


Yoo et al. (US Pub 2002/0161968) describes a memory system having a stub bus configuration.

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Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andrew Q. Tran whose telephone number is (571) 272-1885. The examiner can normally be reached on Mon - Fri 8:30 AM - 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard T. Elms can be reached on (571) 272-1869. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

  
Andrew Q Tran  
Primary Examiner  
Art Unit 2824

at  
May 12, 2006